

CLAIMS

1. Device for comparing two words N and P of n bits each, characterised in that it includes at least one level-1 comparator block which itself includes:

- n basic comparator blocks, each enabling the bits
5 N_i and P_i of position i of words N and P to be compared, with i being between 0 and n-1, and each including:
 - * a first sub-block for generating at its
10 output, forming a first output of the basic comparator block, a first signal indicating whether or not the bits N_i and P_i are equal;
 - * a second sub-block enabling a second signal, indicating which of the bits N_i and P_i is greater, to be generated at its output;
 - 15 * a third sub-block enabling the second signal to pass to a second output of the basic comparator block, if the first signal does not indicate an equality of the bits N_i and P_i , and otherwise enabling the second signal
20 to be blocked;
- means for generating a third signal at a first output of the level-1 comparator block, indicating that the numbers N and P are equal if the n first signals indicate that the n bits N_i and the n bits
25 P_i are equal, and otherwise indicating that the numbers N and P are not equal;
- first selective passage means enabling the second output of a basic comparator block to be selectively connected to a second output of the

level-1 comparator block, which basic comparator block, from among the basic comparator blocks having a second signal at their second output, processes higher-order bits, with the signal present at the second output of the level-1 comparator block indicating which of the numbers N and P is greater.

2. Device according to claim 1, characterised in that the first sub-block includes an "exclusive-OR" gate receiving the bits N_i and P_i at the input.

3. Device according to claim 1, characterised in that the second sub-block includes an "OR" gate receiving, at the input, the bit P_i and, via an inverter, the bit N_i .

4. Device according to claim 1, characterised in that the third sub-block includes a "selective passage" gate of which the input is connected to the output of the second sub-block and which is controlled by the output of the first sub-block.

5. Device according to claim 1, characterised in that the means for generating the third signal, at the first output of the level-1 comparator block, include an "OR" gate of which the inputs are connected to the first outputs of the basic comparator blocks.

6. Device according to claim 1, characterised in that the first selective passage means include:

- means enabling the second output of the basic comparator block processing the high-order bits N_{n-1} and P_{n-1} to be directly connected to the second output of the level-1 comparator block;

- for each of the other basic comparator blocks processing N_j and P_j bits, with j being between 0 and $n-2$, means for connecting the second output of the basic comparator block to the second output of the level-1 comparator block, via a "selective passage" gate (pass-gate) controlled by the output of an "OR" gate of which one inputs are connected to the first outputs of the basic comparator blocks of higher order than j .

7. Device according to claim 1, characterised in that said at least one level-1 comparator block also includes means for storing the value present at the second output of the level-1 comparator block.

8. Device according to claim 7, characterised in that the storage means include:

- a "NOT OR" gate of which a first input is connected to the second output of the level-1 comparator block and a second input is connected, via an inverter, to the first output of the level-1 comparator block;
- a low-current inverter connecting the output of said "NOT OR" gate to the first input of said "NOT OR" gate.

9. Device according to claim 1, characterised in that it includes at least one level-2 comparator block which itself includes:

- q level-1 comparator blocks, with $q \geq 2$, each including a portion of the n basic comparator blocks;
- means for generating a fourth signal at a first output of the level-2 comparator block, indicating

that the numbers N and P are equal if the first outputs of the q level-1 comparator blocks indicate that the bits that they compare are equal, and otherwise indicating that the numbers N and P are not equal;

- second selective passage means, enabling the second output of a level-1 comparator block to be selectively connected to a second output of the level-2 comparator block, which level-1 comparator block, from among the level-1 comparator blocks having a second signal at their second output, processes higher-order bits, with the signal present at the second output of the level-2 comparator block indicating which of the numbers N and P is greater.

10. Device according to claim 9, characterised in that the means for generating the fourth signal, at the first output of the level-2 comparator block, include an "OR" gate of which the inputs are connected to the first outputs of the level-1 comparator blocks.

11. Device according to claims 9 or 10, characterised in that the second selective passage means include:

- means enabling the second output of the level-1 comparator block processing the high-order bits to be connected to the second output of the level-2 comparator block, via a "selective passage" gate controlled by the first output of the level-1 comparator block processing the high-order bits;
- for each of the other level-1 comparator blocks, means for connecting the second output of the

level-1 comparator block to the second output of the level-2 comparator block, via a "selective passage" gate controlled by the output of an "OR" gate of which one input is connected, via an inverter, to the first output of said level-1 comparator block, and of which the other inputs are connected to the first outputs of the higher-order level-1 comparator blocks.

12. Device according to claim 9, characterised in that said at least one level-2 comparator block also includes means for storing the value present at the second output of the level-2 comparator block.

13. Device according to claim 12, characterised in that the storage means include:

- 15 - a "NOT OR" gate of which a first input is connected to the second output of the level-2 comparator block and a second input is connected, via an inverter, to the first output of the level-2 comparator block;
- 20 - a low-current inverter connecting the output of said "NOT OR" gate to the first input of said "NOT OR" gate.

14. Device according to claim 1, characterised in that it includes at least one level-k comparator block, with $k \geq 2$, which itself includes:

- p level-k-1 comparator blocks, with $p \geq 2$;
- means for generating a fifth signal at a first output of the level-k comparator block, indicating that the numbers N and P are equal if the first outputs of p level-k-1 comparator blocks indicate that the bits that they are comparing are equal,

and otherwise indicating that the numbers N and P are not equal;

- third selective passage means, enabling the second output of a level-k-1 comparator block to be selectively connected to a second output of the level-k comparator block, which level-k-1 comparator block, from among the level-k-1 comparator blocks having a signal at their second output, processes higher-order bits, with the signal present at the second output of the level-k comparator block indicating which of the numbers N and P is greater.

15. Device according to claim 1, characterised in that each selective passage gate includes a transistor N mounted parallel with respect to a transistor P.

16. Device according to claim 1, characterised in that it is produced in the form of a wired circuit.